



IRIS

EE Call Letter List  
PhD, 2024 - 25

NITK / EE D / ...1001.....

Subject: Ph.D. Shortlisted Candidates

Date: 08/05/2024

The following applicants have been selected for written exam and/or interview for the department for the department of Electrical and Electronics Engineering for PhD Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	BHUKYA HARI KRISHNA	PH2024EE0001	Electrical and Electronics Engineering
2	BHUKYA HARI KRISHNA	PH2024EE0002	Electrical and Electronics Engineering
3	kamlesh mehar	PH2024EE0003	Electrical and Electronics Engineering
4	SIDDHARTH SEN	PH2024EE0005	Electrical and Electronics Engineering
5	Ranjeet Kumar	PH2024EE0006	Electrical and Electronics Engineering
6	Vidyashankar M	PH2024EE0007	Electrical and Electronics Engineering
7	Lalitha Pai B	PH2024EE0008	Electrical and Electronics Engineering
8	VISHWANATHAN P	PH2024EE0009	Electrical and Electronics Engineering
9	Raghavendra Satalagaon	PH2024EE0010	Electrical and Electronics Engineering
10	Pritam Mandal	PH2024EE0012	Electrical and Electronics Engineering
11	KOSIGI RAMESH	PH2024EE0013	Electrical and Electronics Engineering
12	Vijay R Bagewadi	PH2024EE0014	Electrical and Electronics Engineering
13	Nallagatla Rajesh	PH2024EE0015	Electrical and Electronics Engineering



IRIS

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

राष्ट्रीय प्रौद्योगिकी संस्थान कर्नाटक, सुरत्कल

P.O SRINIVASNAGAR, MANGALORE - 575025

EE Call Letter List

PhD, 2024 - 25

#	Name	Reference Number	Engineering Branch/Specialisation
14	TALAPATI AKHIL SAI	PH2024EE0016	Electrical and Electronics Engineering
15	RASHMI S HUGAR	PH2024EE0017	Electrical and Electronics Engineering
16	ARKO GOSWAMI	PH2024EE0018	Electrical and Electronics Engineering
17	RAJINIKANDH C	PH2024EE0019	Electrical and Electronics Engineering
18	Sharmila Devi S	PH2024EE0020	Electrical and Electronics Engineering
19	VENKATANNA	PH2024EE0021	Electrical and Electronics Engineering
20	VENKATAMAHESHBABU LELLA	PH2024EE0022	Electrical and Electronics Engineering
21	KADAPALA GANGADHAR	PH2024EE0023	Electrical and Electronics Engineering
22	Firdous kahkashan	PH2024EE0024	Electrical and Electronics Engineering
23	CHAITANYA L	PH2024EE0025	Electrical and Electronics Engineering
24	MALLIKARJUN BHAGAWATI	PH2024EE0027	Electrical and Electronics Engineering
25	Dipali Dey	PH2024EE0029	Electrical and Electronics Engineering

 08/05/2024

**Head Of Department**  
**Electrical and Electronics Engineering**

PROFESSOR AND HEAD

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING  
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA  
SRINIVASNAGAR, SURATHKAL, MANGALORE - 575 025, INDIA

1001  
Subject: Ph.D. Shortlisted Candidates  
08/05/2024

**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**  
**NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL,**  
**SRINIVASNAGAR, MANGALORE – 575 025**

Tel : 0824-2473045, 2474054  
Fax : 0824-2474039  
Website : www.eee.nitk.ac.in

Date: 8<sup>th</sup> May 2024

To the shortlisted candidates:

With reference to your application for admission to **Ph.D. Programme in the Department of Electrical and Electronics Engg.**, you are requested to appear physically/online before the selection committee at your own cost for PhD admission selection process. You should produce all records such as Date of Birth Certificate, Degree Certificate, Marks Cards of all years/semesters (U.G. and P.G. Programmes), Class 10<sup>th</sup> & 12<sup>th</sup>, GATE Score Card, Diploma Marks Card, Sponsorship certificate (if applicable), SC/ST Certificate (if applicable), OBC Certificate issued on or after 01 April 2024 (if applicable), EWS Certificate issued on or after 01 April 2024 (if applicable), Persons with Disabilities (PWD) certificate (if applicable), Conduct certificate and Testimonials, and valid photo identity card, (All originals). Please bring a self-attested photocopy of each of these certificates to submit at the time of interview.

Department	: Electrical and Electronics
Place of Interview	: Dept. of Electrical and Electronics Engg., Western Side Campus, NITK, Surathkal
Registration	: 20-05-2024, 08:30 AM at Seminar Hall, Dept. of E & E
Document Verification	: 20-05-2024, 09:00 AM at Seminar Hall, Dept. of E & E
Written Test	: 20-05-2024, 11:00 AM to 12:00 PM at Seminar Hall, Dept. of E & E
Announcement of Shortlisted Candidates for Interview* (provisional; pending document verification)	: 20-05-2024, 01:30 PM
Interview	: 20-05-2024, 02.00 PM to 5:30 PM and 21-05-2024, 09.00 AM onwards at Conference Room, Dept. of E & E

Note:

1. Please see the institute eligibility criteria given in the advertisement, carefully. It is the sole responsibility of the candidate to ascertain his/her eligibility before coming for the interview. The final confirmation of your eligibility is done only after the verification of original certificates.
2. Candidates are required to go through the list of Instructions to Candidates which is enclosed herewith.
3. Candidates must bring the "Data Collection Format" (enclosed) duly filled and submit at the time of registration/verification of documents on 20<sup>th</sup> May 2024.
4. Full-time/External Registrants - sponsored from Industry or other organizations including Educational Institutions, should have been serving in the sponsoring organization for a period of at least 2 years after qualifying degree and have to produce a letter from their employer stating that the candidate is deputed for Research Programme (Full time/Part time) of the Institute on full salary, during the study period. The employer should indicate that the candidate will not be withdrawn midway before the completion of the course. (Sponsorship letter should be in the format provided in the Application Form).
5. Candidates who have not submitted marks of final examination along with application form shall produce the same at the time of admission. However, candidates who have written final year examinations and are yet to obtain final semester mark cards should submit the same on or before 30-09-2024.
6. Candidates who have got the degree(s) from the other Universities (Other than NITK) have to produce Migration certificate in order to validate their admission at a later stage.
7. The Selected candidates are required to pay fees and get admitted to the institute as per dates specified by the institute. Fee details are as given in the "Information Bulletin 2024-25 (M.Tech and PhD)".

  
(HoD & Chairman DRPC, EED)

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**PROFESSOR AND HEAD**

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING  
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA  
SRINIVASNAGAR, SURATHKAL, MANGALORE - 575 025, INDIA

**NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA-SURATHKAL**  
**DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

Date: 8<sup>th</sup> May 2024

**INSTRCTIONS TO CANDIDATES APPLIED FOR Ph.D. PROGRAMME.**

Dear Candidates,

You are invited to participate physically/offline in the selection process of admission to the Ph.D. programme in our department. Here are few more instructions to make it convenient for all of us.

1. The following Certificates shall be brought in ORIGINAL for verification purposes.
  - (a) GATE Score Card
  - (b) B.E / B.Tech and M. Tech/M.E. Marks Cards and Degree Certificates
  - (c) X and XII marks cards
  - (d) Caste Certificate (if applicable)
  - (e) Valid proof of photo identity.

(Note: For OBC, the certificate must be dated on or after 1<sup>st</sup> April 2024. Please make sure that the caste name appear in the central list published by National Commission of Backward Classes (NCBC) Govt. of India at the link: [www.ncbc.nic.in](http://www.ncbc.nic.in). **If the caste is not listed by NCBC or the certificate date is prior to 1<sup>st</sup> April 2024, then the OBC candidate will be considered under Open Category Only.** The OBC certificate format is available through the institute website ([www.nitk.ac.in](http://www.nitk.ac.in)). For EWS Category, the Certificate should be as per prescribed format issued by the Competent Authority on or after 1-4-2024).
2. Please visit the Department Website ([www.eee.nitk.ac.in](http://www.eee.nitk.ac.in)) for updates and instructions which will be released by the department from time to time. The Department will not entertain any such concerns by the candidates regarding unawareness of the updates and instructions published in the department website.
3. Non-Production of Original Documents for Verification Purposes will disqualify the candidate from selection process.
4. The procedure for selection is given on **Pages 3 & 4** of this document. The Candidates are required to go through the procedure carefully before appearing for the selection process.
5. The candidates are informed to download and fill up the Data Collection Format (**Pages 5 to 8**) carefully and submit during Document Verification. This data will be used for preparation of the merit list.
6. The Candidates are required to produce reprints of their publications, original certificates of work-experience and training-undergone at the time of Interview.
7. The Candidates are required to be available on **20<sup>th</sup> May 2024** at Dept. of E & E, NITK, Surathkal for completion of the selection process and be available on mobile call for receiving and providing necessary information.
8. The candidates have to comply with the instructions published in the information bulletin for Ph.D & M.Tech Programme 2024-25, regarding admission procedure as stipulated by the Institute.
9. For any clarifications contact Dr. Tukaram Moger, Secretary, DRPC, through e-mail: [tukaram@nitk.edu.in](mailto:tukaram@nitk.edu.in) or Phone : +91-824-2473451 (Office), +91-9611475268 (Cell).

  
(HoD & Chairman DRPC, EED)  
PROFESSOR AND HEAD

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING  
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA  
SRINIVASHNAGAR, SURATHKAL, MANGALORE - 575 025, INDIA

**Admission to Ph. D. Programme, 2024-25 (July Session): Selection Procedure:**

**Factors considered for selection:** The selection of the scholars is based on all the following components considered at different stages as indicated in the *Procedure of Selection (at the department level)*:

1. Application in the prescribed format with all necessary data and submission of further information/ data sought by the department at the time of registration and interview.
2. Performance in the U.G and P.G. degrees.
3. Performance in the written test.
4. Performance in the technical presentation, and Q&A on technical presentation
5. Performance in the technical interview
6. Experience and publications to be assessed during the interview.

**Procedure of Selection (at the department level): The selection will involve three stages.**

**Stage-1:** All eligible candidates will be allowed to compete in the written test, which is of multiple-choice type questions. **The topics for the written test are the syllabus of GATE (EE-Electrical Engineering) exam.** A short-list of candidates for technical presentation and technical interview will be formed by considering the performance at the UG, PG, and the written test. Cut-off will be decided considering the number of seats permitted by the institute or the capacity of the department whichever is lower, and applying a relaxation for different categories (OBC, SC, ST, and PWD). This is detailed in the *Procedure of short-listing of candidates for PhD admission selection process.*

**Stage-2:** The short-listed Candidates in Stage-1, will be called for technical presentation followed by the Q&A on technical presentation, and then technical interview by the Doctoral Research Programme Committee (DRPC). The DRPC will prepare a list of candidates recommending for admission to Ph.D. programme based on the performance in the technical interview (which includes publications, experience, technical presentation, Q&A on technical presentation, and technical interview) and written test. This list will be submitted to the Head of the Department. This may be a NULL list in case no candidate is found suitable.

Written test	Technical Interview				Total
	Publications	Experience	Technical Presentation	Q&A on Technical Presentation	
40 %	5%	5%	10%	40%	100%

**Stage-3:** The Head of the Department will allocate the candidates to the Faculty members by looking into the candidate's research interest and the research area of Faculty members intending to take the Ph. D. scholars, and forward the recommendation to the Dean (A).

**Procedure of short-listing of candidates for PhD admission selection process:**

**Step-1:** All the Candidates meeting the institute eligibility criteria will be called for participating in the selection process.

**Step-2:** A written test will be conducted on the first day of the process to get a departmental level assessment of the candidates.

**Step-3:** A merit order will be formed for short-listing of candidates for interview giving weightages for different components as follows:

Undergraduate performance (First to final semester)	Postgraduate performance (First to second semester)	Written test	Total
30 %	20 %	50 %	100 %

  
8/08/2024

**Step-4:** If the department has  $N$  number of seats in the Open Category (OC), then the cut-off mark ( $M1$ ) for OC will be the mark of  $(3N)^{th}$  candidate in the merit order formed in Step-3. This list ( $L1$ ) may be represented by the candidates from all categories (OC, EWS, OBC, SC, ST and PWD).

**Step-5:** The cut-off mark ( $M2$ ) for OBC candidates is fixed at 90% of the Cut-off mark ( $M1$ ) for OC. This list is  $L2$  and contains all OBC candidates having score between  $M1$  and  $M2$  (included), but limited by 3 times the number of seats available in OBC category.

**Step-6:** The cut-off mark ( $M3$ ) for SC candidates is fixed at 75% of the Cut-off mark ( $M1$ ) for OC. This list is  $L3$  and contains all SC candidates having score between  $M1$  and  $M3$  (included), but limited by 3 times the number of seats available in SC category.

**Step-7:** The cut-off mark ( $M4$ ) for ST candidates is fixed at 70% of the Cut-off mark ( $M1$ ) for OC. This list is  $L4$  and contains all ST candidates having score between  $M1$  and  $M4$  (included), but limited by 3 times the number of seats available in ST category.

**Step-8:** The shortlist of candidates for the interview is  $L=L1 + L2 + L3 + L4 +$  other student types (full-time/part-time sponsored etc.).

**Guidelines for Technical Presentation during the interview:**

- 1) All the shortlisted candidates are required to give the technical presentation during the interview.
  - 2) Topic for the presentation: Topic of your research interest area.
- Time duration for the presentation: 10 minutes (Maximum 4 slides) followed by Q & A Session.

  
(HoD & Chairman, DRRC, EED)

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NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA  
SRINIVASHNAGAR, SURATHKAL, MANGALORE - 575 025, INDIA

**Data Collection format**

**Admission to Ph.D. Programme, 2024-25 (July Session)**

<b>Name of the Candidate</b>				<b>Application No.</b>			
<b>Email id:</b>				<b>Mobile No.</b>			
<b>PG</b>			<b>Awarded Marks / Grades</b>		<b>Equivalent % age marks</b>		
	PG (up to 2 semesters)	CGPA (C1G)			(C1G-0.5)*10		
		C1=%age			C1		
	PG (Aggregate of all semesters)	CGPA (C2G)			(C2G-0.5)*10		
		C2=%age			C2		
<b>GATE</b> (* Declared out of 100 in GATE score card)		<b>Year</b>		<b>Marks(*)</b>		<b>Marks Normalized(*)</b>	
<b>UG</b> (Degree awarded)		<b>Awarded Marks / Grades (aggregate of 8 semesters)</b>			<b>Equivalent %age Marks (B=)</b>		
		CGPA (C4G)			(C4G - 0.5)*10		
		C4=%age			C4		
<b>10th Level (CGPA/ Marks)</b>				<b>12th level (CGPA/ Marks)</b>			
<b>Diploma (CGPA/ Marks)</b>							
<b>Remarks (CGPA of 6.0/60%) (CGPA 5.5/55%: SC/ST/PWD)(@ PG levels)</b>		<b>QUALIFIED</b>		<b>NOT QUALIFIED</b>			
<b>Experience and Publications to be considered during the interview.</b>							
<b>Experience (in years)</b>	<b>Teaching</b>		<b>Industry</b>		<b>Others (Specify)</b>		<b>Remarks</b>
<b>Publications (Numbers)</b>	<b>Journals</b>		<b>Conferences</b>		<b>Books</b>		<b>Remarks</b>

Declaration by the Candidate:

I hereby state that I have understood all the instructions provided so far and that I have taken all the necessary care in providing the information in the Data Collection Form. I will be solely responsible for all the consequences arising out of submission of incorrect data, the one that is being used in the selection process.

Signature of the candidate  
Date: 20-05-2024  
Place: NITK, Dept. of EE

Verified by: Signature  
Name:  
Designation: Faculty Member/ Staff

# PG- Degree

Name of the candidate							Application No.						
Semester	Course Details			Result			Semester	Course Details			Result		
	Course code	Credits	Max. Marks/	Grade	Point	Marks		Course code	Credits	Max. Marks/	Grade	Point	Marks
1							2						
3							4						
CGPA (in case of Grades) upto 2nd Semester				CIG		CGPA (in case of Grades) upto 4th Semester				C2G			
Percentage (in case of Marks) upto 2nd Semester				C1		Percentage (in case of Marks) upto 4th Semester				C2			

Signature of the Candidate:  
 Date: 20-05-2024  
 Place: NITK, Dept. of EE

Verified by: Signature  
 Name:  
 Designation: Faculty Member/ Staff



**UG (Semesters 1 to 4) (First Attempt Grades/ Marks only to be used)**

Name of the candidate							Application No						
Sem.	Course Details			Results			Sem.	Course Details			Results		
	Course Code	Credits	Max. Marks	Grade	Grade Point	Marks		Course Code	Credits	Max. Marks	Grade	Grade Point	Marks
1							2						
3							4						

Signature of the candidate  
 Date: 20-05-2024  
 Place: NITK, Dept. of EE

Verified by: Signature  
 Name:  
 Designation: Faculty Member/ Staff

**UG (Semesters 5 to 8) (First Attempt Grades/ Marks only to be used)**

Name of the candidate							Application No						
Sem.	Course Details			Results			Sem.	Course Details			Results		
	Course Code	Credits	Max. Marks	Grade	Grade Point	Marks		Course Code	Credits	Max. Marks	Grade	Grade Point	Marks
5							6						
7							8						

Signature of the candidate  
 Date: 20-05-2024  
 Place: NITK, Dept. of EE

Verified by: Signature  
 Name:  
 Designation: Faculty Member/ Staff